

### **REMARKS**

Claims 1-29 are pending in the application. Reconsideration of claims 1-29 in light of the arguments and amendments herein is respectfully requested.

#### **Allowable Subject Matter**

Claims 1-21 stand allowed. Accordingly, only claims 22-29 remain at issue.

#### **Prior Art Rejection**

Claims 22-29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Oshima et al., Patent Publication no. US 2001/0052093 A1, published on December 13, 2001 ("Oshima"). Reconsideration of this rejection is respectfully requested.

Oshima discloses a tester for a memory. The memory cells are arranged in blocks and address lines. The cells of one block share a common row address. The cells of one address line share a common column address.

The disclosed tester comprises a circuit 202 for detecting bad blocks, a circuit 203 for detecting bad address lines and a circuit 204 for detecting whether the memory is bad. Each of these circuits comprises one of the cited comparators CP1, CP2 and CP3 and a respective one of cited registers RG1, RG2 and RG3. Each of the registers RG1, RG2 and RG3 stores a predetermined number. For example, the register RG1 stores the number of spare address lines plus one and the register RG2 stores the number of spare blocks plus one.

In contrast, the present application defines a memory having a built in self test circuit with a register stack for storing the n highest fail counts and the respective addresses. The stack is operable to accept a new fail count and respective addresses stored in an input register only if at least one address having a lower fail count is found).

Two embodiments are specified with reference to figures 2 and 3. In the first embodiment, the circuit comprises one comparator and one switch for each of the slots of the register stack. The fail count stored in the input register is simultaneously compared to all of the fail counts stored in the slots of the register stack. In the second embodiment, the circuit

comprises just a single comparator and a single switch. The stack is operable to rotate the stored fail counts and respective addresses.

By this paper, claims 22, 24 and 26-29 have been amended to clarify the invention defined by these claims. First, independent claim 22 has been amended to recite "A memory device having a built in self test circuit." As noted above, Oshima actually relates to a tester for a memory, not a memory device itself. As such, Oshima includes "a testing apparatus proper (hereinafter, referred to as a main frame) 200 called "main frame" in this technical field, and a test head 300." Oshima, ¶[0053]. Clearly, Oshima discloses equipment which is substantially different in construction and content from the memory device of claim 22.

Second, independent claims 22 and 29, as amended, are clearly distinguishable over Oshima. Claim 22 recites that the memory device includes a plurality of comparators. Each comparator is coupled to the input register to receive the input fail count and coupled to a slot of the register to receive a stored fail count from the slot. Further, each comparator compares the input fail count and the fail count and, when the input fail count exceeds the fail count, the input fail count is transferred from the input register. Similar amendments have been made to claim 29 to more clearly recite a distinct memory device.

Oshima fails to disclose comparable structure. The office action refers to comparators CP1, CP2 and CP3 of Oshima as corresponding to the claimed plurality of comparators. However, Oshima FIG. 2 makes clear that CP1, CP2 and CP3 are not coupled to the input register and one of the slots of the register, as in claims 22 and 29. In the office action, register RG1 of Oshima is assigned to be both the register and the input register. No separate register is identified. Clearly, Oshima fails to disclose all of the claimed structure or claimed operation of claims 22 and 29.

Claims 24 and 26-28 have been similarly amended to more clearly recite the structure of the claimed invention. Oshima fails to disclose the structure defined by these claims, as well.

Accordingly, it is respectfully submitted that independent claims 22 and 29 are allowable over the cited reference. Claims 23-28 are dependent from claim 22 and add further limitations thereto, and are allowable for the same reason. Withdrawal of the 35 U.S.C. § 102(a) rejection of claims 22-29 is respectfully requested.

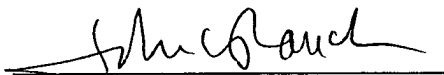
Application no. 10/624,031  
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Claim Objections

Claim 7 stands objected to under 37 C.F.R. § 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim. By this paper, claim 7 has been amended to change its dependency to claim 6. Withdrawal of the objection is respectfully requested.

With this response, the application is believed to be in condition for allowance. Should the examiner deem a telephone conference to be of assistance in advancing the application to allowance, the examiner is invited to call the undersigned attorney at the telephone number below.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "John G. Rauch", is written over a horizontal line.

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